THAT WHICH IS CLAIMED IS:

1. A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein;

wherein t is a thickness of the semiconductor wafer, ϕ_1 is an angle in a range between about 30° and about 85°, R is a radius of an arc that defines EP_{in} at a point of intersection with a top surface of the semiconductor wafer, and α is an acute angle that represents an angle of intersection between a bottom surface of the semiconductor wafer and a line that is tangent to the arc at a point on EP_{out}; and

wherein:

$$A_1=R(1-\cos\phi_1);$$

$$A_2=R(1-\sin\alpha) + (t-R\sin\phi_1 - R\cos\alpha)\cot\alpha;$$

$$B_1=R\sin\phi_1; \text{ and}$$

$$B_2=t-R\sin\phi_1.$$

2. The wafer of Claim 1, wherein R is in a range between about 0.23t and about 0.5t.

3. The wafer of Claim 2, wherein A_2 is greater than about two times A_1.

4. The wafer of Claim 2, wherein ϕ_1 is in a range between about 60° and about 75°.

5. The wafer of Claim 2, wherein t is in a range between about 625 μm and about 825 μm.

6. A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein; wherein ϕ_1 is an angle in a range between about 30° and about 85°; and wherein R is in a range between about 0.23t and about 0.5t.

7. The wafer of Claim 6, wherein A_2 is greater than about two times A_1.

8. The wafer of Claim 6, wherein ϕ_1 is in a range between about 60° and about 75°.

9. The wafer of Claim 6, wherein t is in a range between about 625 μm and about 825 μm.

10. A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein.

11. A semiconductor wafer having an asymmetric edge profile that consists of an arc, which has a radius R that sweeps a downward angle of 2ϕ from a top surface of the wafer, and a straight line that is orthogonal to R and extends from one end of the arc to a bottom surface of the wafer.

12. The wafer of Claim 11, wherein ϕ is in a range between about 60° and about 75°.

13. The wafer of Claim 12, wherein t, a thickness of the wafer, is in a range between about 625 μm and about 825 μm.

14. The wafer of Claim 13, wherein R is in a range between about 0.23t and about 0.5t.

15. A method of forming a semiconductor wafer, comprising the steps of:

slicing a semiconductor ingot into at least one semiconductor wafer having a top surface and a bottom surface; and

grinding a peripheral edge of the at least one semiconductor wafer to define an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein.

16. The method of Claim 15, wherein said grinding step is followed by the step of polishing the top surface of the semiconductor wafer.

17. The method of Claim 15, wherein said grinding step is followed by the step of polishing the top surface of the semiconductor wafer to define an asymmetric edge profile EP2 extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein.

18. A semiconductor wafer having an asymmetric edge profile (EP2) extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein; wherein ϕ_1 and ϕ_2 are angles in a range between about 30° and about 85° ; wherein $\phi_1 < \phi_2$; and wherein R is in a range between about 0.23t and about 0.5t.

19. A semiconductor wafer having an asymmetric edge profile (EP2) extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein;

wherein t is a thickness of the semiconductor wafer, ϕ_1 is an angle in a range between about 30° and about 85°, ϕ_2 is greater than ϕ_1 and less than about 85°, R is a radius of an arc that defines $EP2_{in}$ at a point of intersection with a top surface of the semiconductor wafer, and α is an acute angle that represents an angle of intersection between a bottom surface of the semiconductor wafer and a line that is tangent to the arc at a point on $EP2_{out}$; and

wherein:

$$A_1=R(1-\cos\phi_1);$$

$$A_2=R(1-\sin\alpha) + (B_2 - R\cos\alpha)\cot\alpha;$$

$$B_1=R\sin\phi_1; \text{ and}$$

$$B_2=t-R\sin\phi_1.$$

20. A method of forming a semiconductor wafer, comprising the steps of:

slicing a semiconductor ingot into at least one semiconductor wafer having a top surface and a bottom surface; and

grinding a peripheral edge of the at least one semiconductor wafer to define an asymmetric edge profile (EP2) extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein; wherein ϕ_1 is an angle in a range between about 30° and about 85°; and wherein ϕ_2 is an angle that is greater than ϕ_1 and less than about 85°.